TABLE I
MEASUREMENT PERFORMANCES OF NONSATURATED AMPLIFIERS
($V_{DD} = 5$ V, $V_{SS} = -5$ V, $C_L = 15$ pF)

Parameter		Measured Values		Units
		2-stage Amp	Transconductance Amp	
Input offset voltage		11	8	mV
DC open loop gain		73	51	dB
Unity gain frequency		7.5	3.8	M Hz
Phase margin		50	80	degree
PSRR @50 K Hz	(V_{DD})	71	-	dB
	(V_{SS})	57	-	
Slew rate Unity gain $V_{in} = \pm 2$V	Rising	60	18	V/μS
	Falling	1.0	20	
DC Power dissipation*		1.0	1.0	mW

* Adjusted by the externally applied biasing voltage during the experiments.

open-loop second pole being located at 90 MHz. The simulated settling characteristics using the SPICE3 and HSPICE circuit simulators [6], [7] are shown in Fig. 2. By increasing output voltage swing, the settling time of an amplifier with the conventional differential input stage increases due to the small input dynamic range. However, the settling time of an amplifier with the nonsaturated input stage is quite independent of the amplifier output voltage swing. The simulated settling time dependence on the feedback factor is shown in Fig. 2(c). It agrees well with the theoretical calculation results using the two-pole method.

Fig. 3 shows a typical bottom-plate switched-capacitor integrator. The output error voltage, which is the difference between the steady-state value and the transient output voltage at a given clocking frequency, is simulated using the amplifiers in Fig. 2(a). As the clocking frequency increases beyond about 200 kHz, the error voltage increases. The output error voltage of an amplifier with the conventional input stage is a strong function of the switching frequency and the output voltage values.

Two amplifiers have been implemented using the proposed design techniques and fabricated in the scalable 2-μm MOSIS technology [8]. The circuit schematics of transconductance amplifier and two-stage CMOS amplifier are shown in Figs. 2(a) and 4(a), respectively. In Fig. 4(a), the bias for cascode structure M_7 and M_8 of the two-stage amplifier is tied to the current-mirror biasing. Since the impedance at the gate electrode of M_7 is very small ($\approx 2g_{m7}$), the gate bias of transistors M_7 and M_8 in the new cascode circuit can be considered as being ac grounded. Transistor M_{13}, which cuts the feedforward signal path from V_{DD} to V_{out}, is biased in the symmetrical manner with respect to transistor M_{14}. The symmetrical circuit structure can minimize the systematic input offset voltage. Measured results are summarized in Table I. The relatively high input offset voltage is caused by the increased number of transistors in the nonsaturated input stage. The high-frequency PSRR characteristics of the two-stage amplifier have been greatly improved. Fig. 5 shows the measured pulsed responses. In the buffer case, the two-stage amplifier output is unsymmetrical because the falling edge is determined by the bias current of the amplifier output stage. In the 17-dB gain case, the amplifier output behaves like an *RC* integrator due to the existence of large phase margin. The response time is independent of the output swing level.

ACKNOWLEDGMENT

The authors would like to thank the reviewers for valuable comments and suggestions.

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A High-Selectivity Continuous-Time GaAs Balanced Filter

YANNICK DEVILLE

***Abstract*—This paper presents a second-order bandpass-like *RC* active filter implemented in 1-μm-gate-length GaAs technology. This filter is designed in order to achieve low sensitivity and high selectivity at the highest possible center frequency. Its quality factor can be tuned up to 20 or 30, using low-accuracy tuning biases, while its center frequency is tuned up to 1.6 GHz.**

I. INTRODUCTION

The few studies of microwave active filters that have been reported involve special structures, such as distributed filters [1] or use of dielectric resonators [2]. However, GaAs microwave monolithic integrated circuits (MMIC's) can be considered as made up of lumped elements up to 5 GHz typically, since their components are located at small distances from one another. Therefore, in this paper we investigate how the MMIC technology can be used to design second-order bandpass-like *RC* active filters having a center frequency above 1 GHz. Only low-gain amplifiers are available in this frequency domain; therefore, classical high-performance low-center-frequency *RC* active filters, based on operational amplifiers, cannot be used here. Besides, classical structures based on low-gain amplifiers, such

Manuscript received September 19, 1989; revised January 8, 1990.
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IEEE Log Number 9035354.

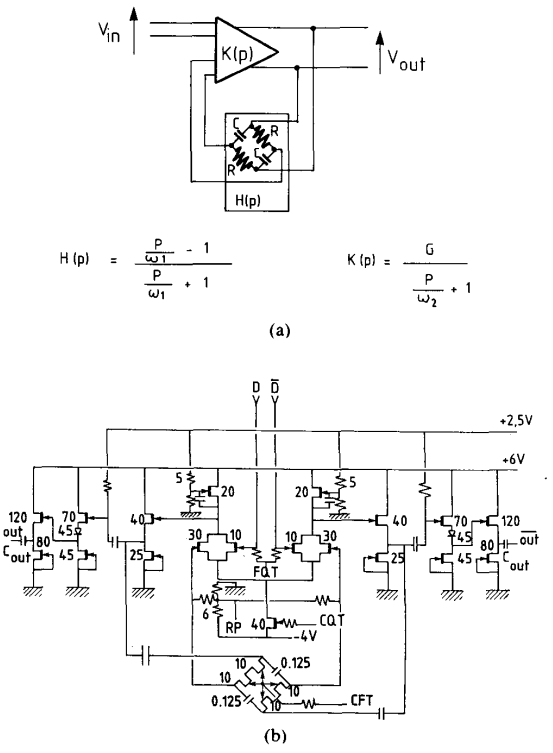

Fig. 1. (a) Proposed structure. (b) Test circuit. The width of transistors and diodes is given in micrometers in the figure. Resistances are 10 kΩ, except values given in kilohms. Capacitances are 1 pF, except values given in picofarads and $C_{out} = 50$ pF.

as Sallen and Key filters [3], will not be used for two reasons. First, their quality factor is highly sensitive to parameter tolerances when it has a high value, as will be discussed further. Instead, the proposed structure yields lower sensitivity. Second, the low-gain amplifier is used here close to its cutoff frequency and thus creates an important phase delay. If a classical structure was used, this phase delay would not be taken into account and the center frequency would be notably lower than expected. Since our first goal is to design a high-selectivity filter having the highest possible center frequency, we will use a structure in which the cutoff frequency of the amplifier is taken into account.

II. Proposed Structure

The structure considered in this paper is shown in Fig. 1(a). The cutoff of the amplifier is taken into account by assuming that its transfer function is of the first-order low-pass type (see $K(p)$ in Fig. 1(a)). We will show in the next section that this assumption is verified in implementations. The proposed structure has the following transfer function:

$$F(p) = \frac{V_{out}}{V_{in}} = \frac{G}{G+1} \cdot \frac{\dfrac{P}{\omega_1} + 1}{\left(\dfrac{P}{\omega_p}\right)^2 + \dfrac{1}{Q} \cdot \dfrac{P}{\omega_p} + 1} \tag{1}$$

with

$$\omega_p = \sqrt{\omega_1 \cdot \omega_2} \cdot \sqrt{G+1} \tag{2}$$

$$Q = \frac{\sqrt{\omega_1 \cdot \omega_2}}{\omega_1 + (1-G) \cdot \omega_2} \cdot \sqrt{G+1}\,. \tag{3}$$

The bandpass and low-pass transfer functions that make up $F(p)$ have the same characteristic frequency f_p. Therefore, $F(p)$ has a second-order bandpass-like response around the center frequency f_p, i.e., it presents a single peak. The characteristic angular frequency ω_1 of the block $H(p)$ is adjusted in order to tune the center frequency of the filter. The cutoff angular frequency ω_2 of the amplifier is a fixed parameter; its low-frequency gain G can be adjusted from zero to its maximum value G_{max} in order to tune the quality factor of the filter. Equation (3) shows that a high-quality factor is obtained by increasing G until the difference at the denominator of Q is low enough. However, if ω_1 is made too high, the filter cannot be selective, since G is limited to G_{max}. Therefore, the "useful band" of the filter, that is, the band of center frequencies at which the filter can be selective, has an upper limit.

An "intermediate" structure will now be considered in order to show that classical filters based on low-gain amplifiers yield lower performance than the proposed structure. The intermediate structure is identical to Fig. 1(a) but uses a high-pass cell:

$$H(p) = \frac{\dfrac{P}{\omega_1}}{\dfrac{P}{\omega_1} + 1}\,. \tag{4}$$

Some (Sallen and Key) classical filters have the same equations as the intermediate structure. However, their first-order low-pass transfer function $K(p)$ is performed by a passive network, while the cutoff of their amplifier is not taken into account and degrades the performance at high frequencies. Therefore, they yield a lower useful band than the intermediate structure, and in this limited band both exhibit the same sensitivity of quality factor to parameter tolerances. The intermediate structure itself provides a lower useful band and higher sensitivity of quality factor to the gain G than the proposed structure. This lower useful band comes from the fact that the center frequency and quality factor of the intermediate structure have the same expression as in (2) and (3), except that they do not contain the term $\sqrt{G+1}$. Therefore, both parameters are lower than for the proposed structure when the same ω_1, ω_2, and G are assumed for both filters. The higher sensitivity of the quality factor of the intermediate structure to the gain G results from the fact that this quality factor does not contain the term $\sqrt{G+1}$: to achieve the same value of quality factor as with the proposed structure, the quality factor of the intermediate structure has a lower denominator and is thus more sensitive to the tolerances of G [4].

III. Chip Implementation

The major part of the test circuit that has been fabricated is shown in Fig. 1(b). This test circuit also contains two differential input stages (not shown) that perform input matching and create the signal $D-\bar{D}$ having very low common mode. This signal is applied to the input of the filter (Fig. 1(b)), whose amplifier is made up of a two-input differential stage, followed by a buffer

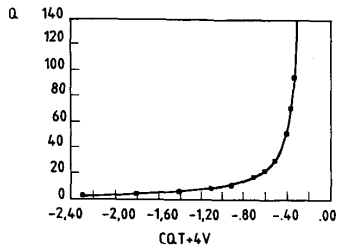

Fig. 2. Tuning of the quality factor Q of the filter by means of the CQT bias. Center frequency is 1.4 GHz.

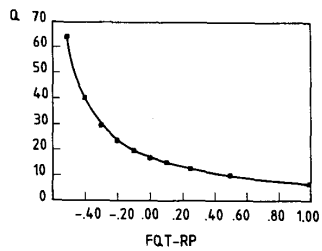

Fig. 3. Tuning of the quality factor Q of the filter by means of the FQT bias (referenced to the reference potential, see text). Center frequency is 1.4 GHz.

stage on each output node. The buffer stages have a much higher cutoff frequency than the differential stage, so that the transfer function of the whole amplifier can be considered to be almost of the first-order low-pass type in the frequency domain of interest, as was assumed in the previous section. The low-frequency gain G, between the input of the differential stage connected to the block $H(p)$ and the output of that stage, can be tuned by two means. First, the bias coarse-Q-tuning (CQT) adjusts the current in that stage and achieves a "coarse" tuning (if compared to the second one) of the gain G and of the quality factor Q. Secondly, the bias fine-Q-tuning (FQT) changes the way this current is split between the two inputs of that stage and provides a finer tuning. The resistors of the RC bridge are each implemented by two transistors in the ohmic mode. The bias center-frequency-tuning (CFT) varies the bias V_{GS} of these transistors, and hence their resistance and the angular frequencies ω_1 and ω_p. The reference potential of the node RP is used as a reference for the biases FQT and CFT. Output impedance matching is achieved by the two buffer stages that are cascaded at each of the outputs nodes of the filter. The capacitors C_{out} are not included on the chip.

IV. Experimental Results

Test chips have been processed using 1-μm-gate-length GaAs MESFET's. Their center frequency can be tuned from about 400 MHz up to slightly more than 2 GHz. However, their useful band is limited to 1.6 GHz. The tuning of the quality factor by use of the biases CQT and FQT is represented in Figs. 2 and 3, respectively. The first tuning bias provides values of the quality factor up to 20 typically, without requiring an accurate control of that bias. Also using the second bias makes it possible to achieve values up to 30 typically, again without requiring an accurate bias. If more accurate biases are used, values above 50 can be achieved.

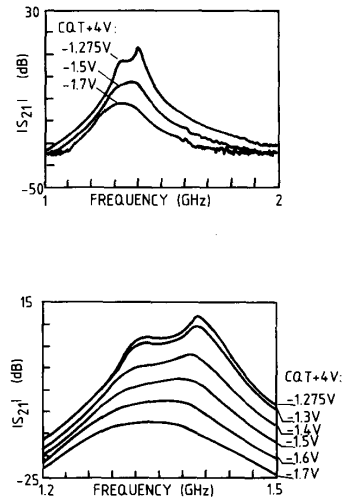

Fig. 4. Transfer function of the cascade connection of two test chips, for various values of the CQT bias.

The chip gain increases with the quality factor Q and is equal to 15 dB when $Q = 20$. Output matching is degraded when the quality factor is increased: a peak appears at the center frequency in the curve of S_{22}, because the output impedance of the filter, which is presented to the output buffer, is modified. However, this effect can be neglected: even when the quality factor is as high as 70, S_{22} remains lower than -10 dB. Other features include a power consumption of 200 mW for the filter and 600 mW for the input/output stages. It should be noted that if the filter is used as an internal block of MMIC's based on lumped elements, the input/output stages will be removed. This will strongly decrease the power consumption and the circuit gain will increase since buffer losses will be avoided.

Fig. 4 shows the transfer functions obtained by cascading two test chips from the same wafer and using the same tuning biases from both chips. The emergence of two peaks for high selectivities is an indication of the on-wafer reproducibility of the technology used.

V. Conclusion

MMIC's make it possible to design high-selectivity second-order RC active filters having a center frequency above 1 GHz: a maximum value of 1.6 GHz is achieved by the structure proposed in this paper, when 1-μm-gate-length MESFET's are used. The availability of only low-gain amplifiers in this frequency domain results in the same sensitivity problems as those that were encountered at low frequencies when designing high-selectivity active filters before the emergence of operational amplifiers. However, the proposed structure possesses improved sensitivity performance and its quality factor can thus be tuned up to 20 or 30 without requiring especially accurate tuning biases, and above 50 if more accurate biases are used. It would be desirable to avoid the need to tune the chips individually. Automatic tuning performed by on-chip master–slave structures has been used in low-frequency filters [5]. These methods involve phase-locking techniques. They would require special care if used here, since the structure presented in this paper does not create a 0 or 90° phase shift at its center frequency. Besides, they would add a significant amount of circuitry to the filter.

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